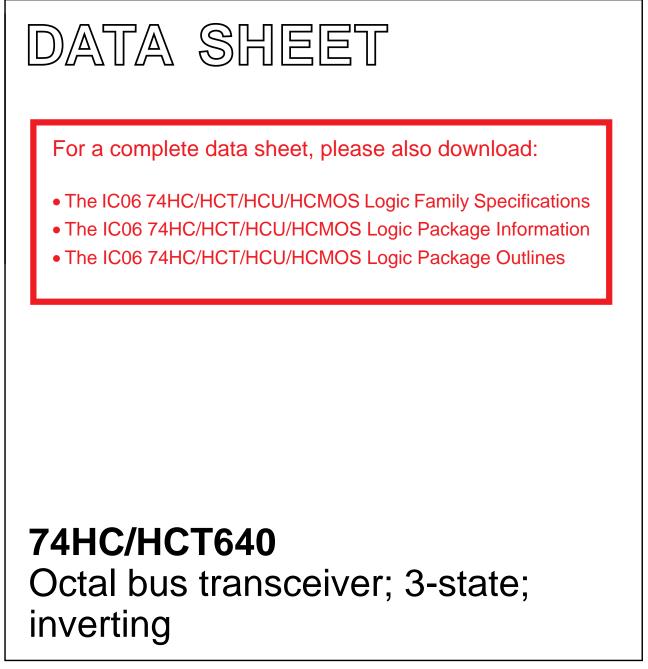
INTEGRATED CIRCUITS



Product specification File under Integrated Circuits, IC06 March 1988



74HC/HCT640

FEATURES

- Octal bidirectional bus interface
- Inverting 3-state outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT640 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT640 are octal transceivers featuring inverting 3-state bus compatible outputs in both send and receive directions.

The "640" features an output enable (\overline{OE}) input for easy cascading and a send/receive (DIR) for direction control. \overline{OE} controls the outputs so that the buses are effectively isolated. The "640" is similar to the "245" but has inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25 \text{ °C}$; $t_r = t_f = 6 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYP	PICAL	UNIT	
STMBOL	PARAMETER	CONDITIONS	нс	нст		
t _{PHL} / t _{PLH}	propagation delay A_n to B_n ; B_n to A_n	C _L = 15 pF; V _{CC} = 5 V	9	9	ns	
CI	input capacitance		3.5	3.5	pF	
C _{I/O}	input/output capacitance		10	10	pF	
C _{PD}	power dissipation capacitance per transceiver	notes 1 and 2	35	35	pF	

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz

 $f_o = output frequency in MHz$

 $\Sigma (C_L \times V_{CC}^2 \times f_o) = sum of outputs$

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

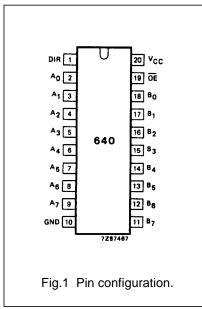
2. For HC the condition is $V_I = GND$ to V_{CC} For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5$ V

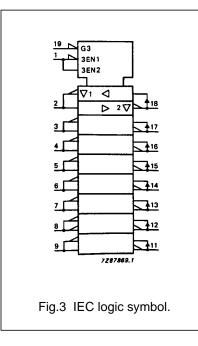
ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION					
1	DIR	direction control					
2, 3, 4, 5, 6, 7, 8, 9	A ₀ to A ₇	data inputs/outputs					
10	GND	ground (0 V)					
18, 17, 16, 15, 14, 13, 12, 11	B ₀ to B ₇	data inputs/outputs					
19	OE	output enable input (active LOW)					
20	V _{CC}	positive supply voltage					





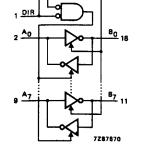


Fig.2 Logic symbol.

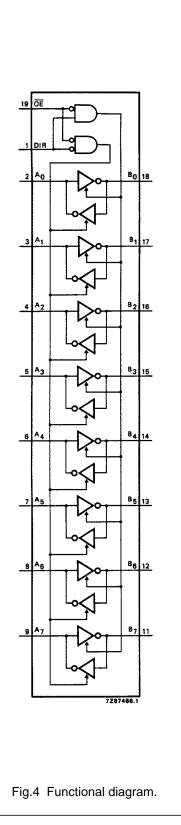
FUNCTION TABLE

19 ÖE

in	outs	inputs/outputs				
OE	DIR	A _n	B _n			
L	L	A=B	inputs			
L	Н	inputs	B=A			
Н	Х	Z	Z			

Note

- 1. H = HIGH voltage level
 - L = LOW voltage level
 - X = don't care
 - Z = high impedance OFF-state



74HC/HCT640

74HC/HCT640

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

SYMBOL	PARAMETER	T _{amb} (°C)								TEST CONDITIONS	
		74HC									
		+25			-40 to +85		-40 to +125		UNIT	V _{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		(,,,	
t _{PHL} / t _{PLH}	propagation delay		30	90		115		135	ns	2.0	Fig.5
	A _n to B _n ;		11	18		23		27		4.5	
	B _n to A _n		9	15		20		23		6.0	
t _{PZH} / t _{PZL}	3-state output enable time		44	150		190		225	ns	2.0	Fig.6
	\overline{OE} , DIR to A _n ;		16	30		38		45		4.5	
	OE, DIR to B _n		13	26		33		38		6.0	
t _{PHZ} / t _{PLZ}	3-state output disable time		50	150		190		225	ns	2.0	Fig.6
	\overline{OE} , DIR to A _n ;		18	30		38		45		4.5	
	OE, DIR to B _n		14	26		33		38		6.0	
t _{THL} / t _{TLH}	output transition time		14	60		75		90	ns	2.0	Fig.5
			5	12		15		18		4.5	
			4	10		13		15		6.0	

74HC/HCT640

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT						
A _n	1.50						
Bn	1.50						
	1.50						
DIR	0.90						

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

SYMBOL		T _{amb} (°C) 74HCT								TEST CONDITIONS	
	PARAMETER										
		+25		-40 to +85		-40 to +125		UNIT	V _{CC} (V)	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay A _n to B _n ; B _n to A _n		11	22		28		33	ns	4.5	Fig.5
t _{PZH} / t _{PZL}	$\begin{array}{l} \textbf{3-state output enable time}\\ \overline{\text{OE}}, \text{ DIR to } A_n;\\ \overline{\text{OE}}, \text{ DIR to } B_n \end{array}$		18	30		38		45	ns	4.5	Fig.6
t _{PHZ} / t _{PLZ}			19	30		38		45	ns	4.5	Fig.6
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.5

va (1)

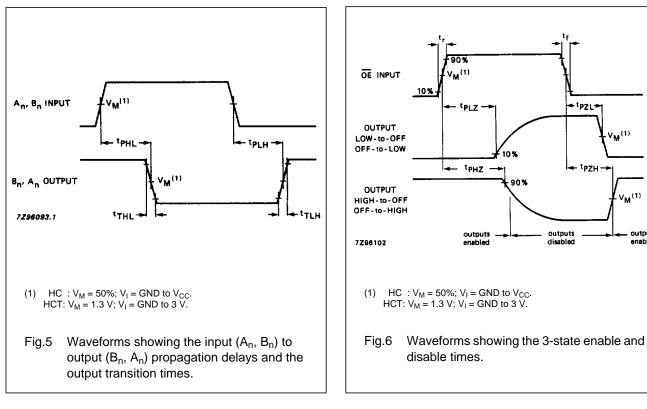
V_M(1)

outputs enabled

Octal bus transceiver; 3-state; inverting

74HC/HCT640

AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".